DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

BY

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16. Abstract

The work on the Process Analysis Structure (PAS) was continued this quarter with the layout being completed, the 100X and 10X artwork being finalized, and the process and test sequences being prepared. Test programs were written for computer-controlled integrated-circuit testing and data reduction.

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SUMMARY

The work on the Process Analysis Structure (PAS) was continued this quarter with the layout being completed, the 100X and 10X artwork being finalized, and the process and test sequences being prepared. Test programs were written for computer-controlled integrated-circuit testing and data reduction.

I. INTRODUCTION

The basic concepts of process evaluation and analysis have been described in previous quarterly reports (No. 18 and No. 19). In general, it has been shown that each process step must be analyzed independently; once this has been done, the interaction between steps can be examined. A carefully designed "Process Analysis Structure" (PAS) can be used for this purpose.

During the third phase of this program the structure was laid out in detail, 100X and 10X artwork was generated, and process sequences were prepared. In addition, test programs were written in preparation for computer-controlled integrated-circuit testing and data reduction. This report, therefore, contains a detailed description of the PAS as well as process listings and testing sequences.

II. PROCESS ANALYSIS AND STRUCTURE

The first mask level is called the silicon island array (Mask #1) and is shown in Fig. 1. The level contains an array of silicon islands which have the following dimensions:

0.2 mil x 200 mils
0.2 mil x 400 mils
0.2 mil x 600 mils
0.2 mil x 1200 mils
0.2 mil x 2400 mils
0.2 mil x 4800 mils

This level contains probing pads to permit evaluation independent of other levels. In addition, there is a second array of silicon islands which is not connected to pads and will be used in conjunction with future levels to check the integrity of contact openings.

The second mask level is shown in Fig. 2 and has been titled the polysilicon array. This level contains strings of polycrystalline silicon which have the following dimensions:

0.2 mil x 400 mils
0.2 mil x 800 mils
0.2 mil x 1200 mils
0.2 mil x 2400 mils
0.2 mil x 4800 mils
0.2 mil x 9600 mils

As can be seen in the illustration, the polysilicon level is a "square wave" pattern and also contains pads for independent probing. An additional polysilicon array is present on this mask level and is interdigitated in the silicon island array for later use in contact evaluation.

The contact array makes up the third mask level and is shown in

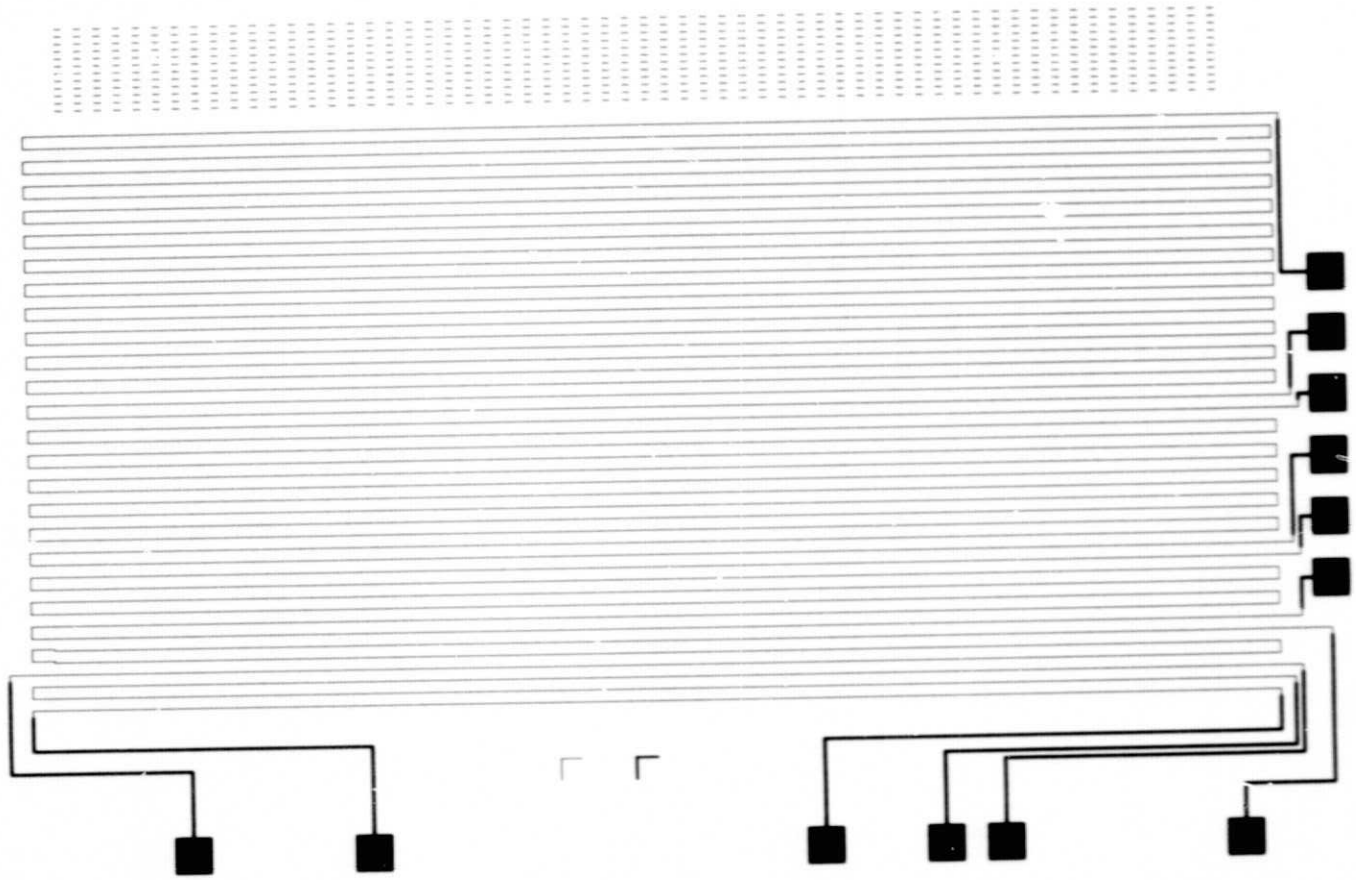

Figure 1. Silicon island array.

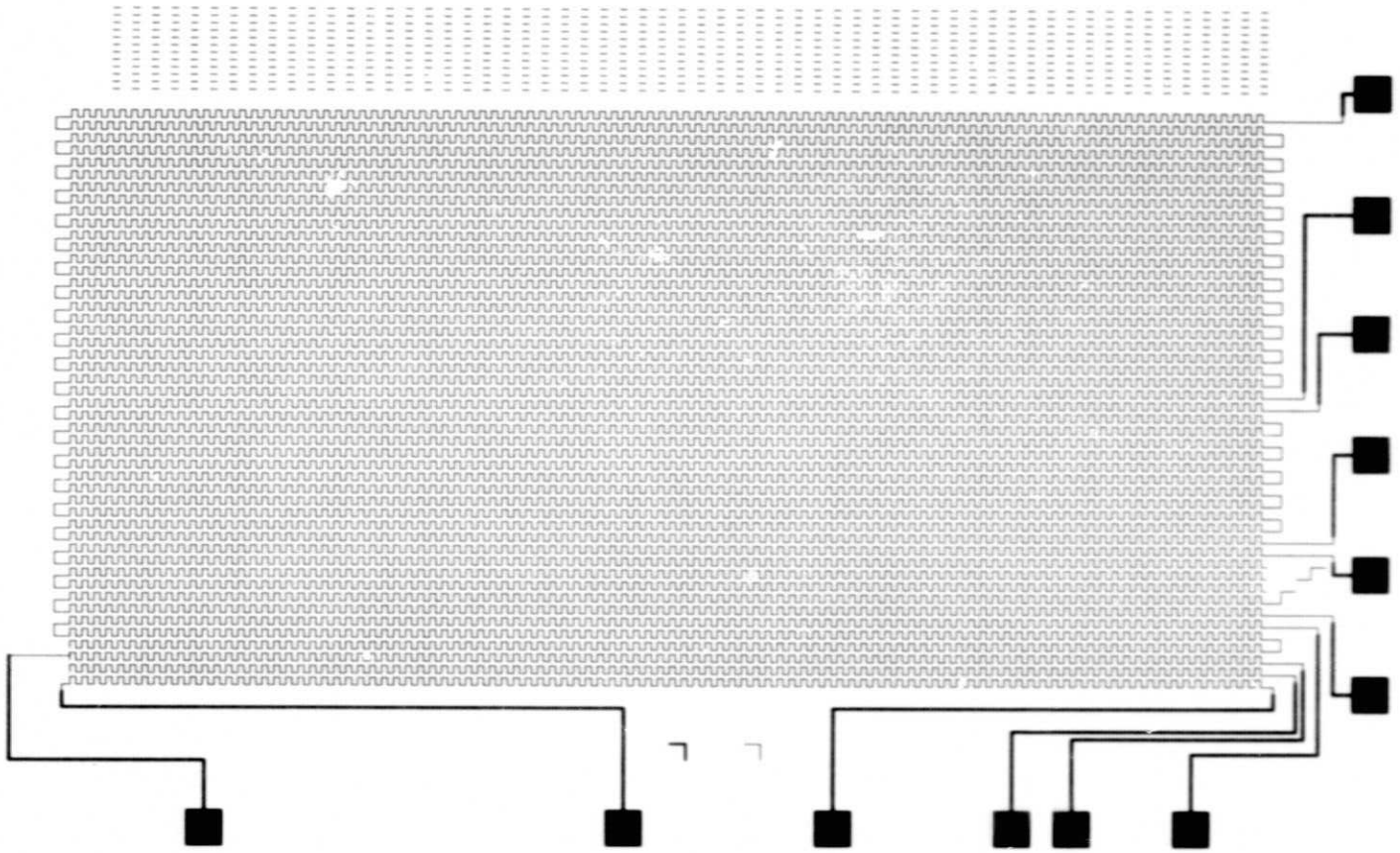

Figure 2. Polysilicon array.

Fig. 3. Again, two distinct arrays are apparent. The larger contact array is used in conjunction with the other levels to check for contact interaction while the smaller array is used to check for contact integrity. All contacts have the dimensions of 0.2 mil by 0.4 mil. The number of contacts which must be opened in the smaller array are:

480 contacts
1440 contacts
2880 contacts

The continuity of this smaller array will depend mainly on the ability of the photoresist and etching characteristics to properly define and open contacts.

The metal pattern is shown in Fig. 4. The large array contains metal lines having the following lengths:

200 mils
400 mils
600 mils
1200 mils
2400 mils
4800 mils

The width of the metal lines is 0.6 mil over the contact openings and 0.4 mil over the polysilicon lines. The smaller metal array connects the silicon islands and polycrystalline silicon together to check the contact opening integrity. This level also places metal over all pads for improved probing.

There is an additional level (Mask #5), called the band pad mask, which simply contains 4-mil squares at the probe pad locations. This mask level is used to open the pad areas only for external probing and can be used to define metal in the probe pad areas.

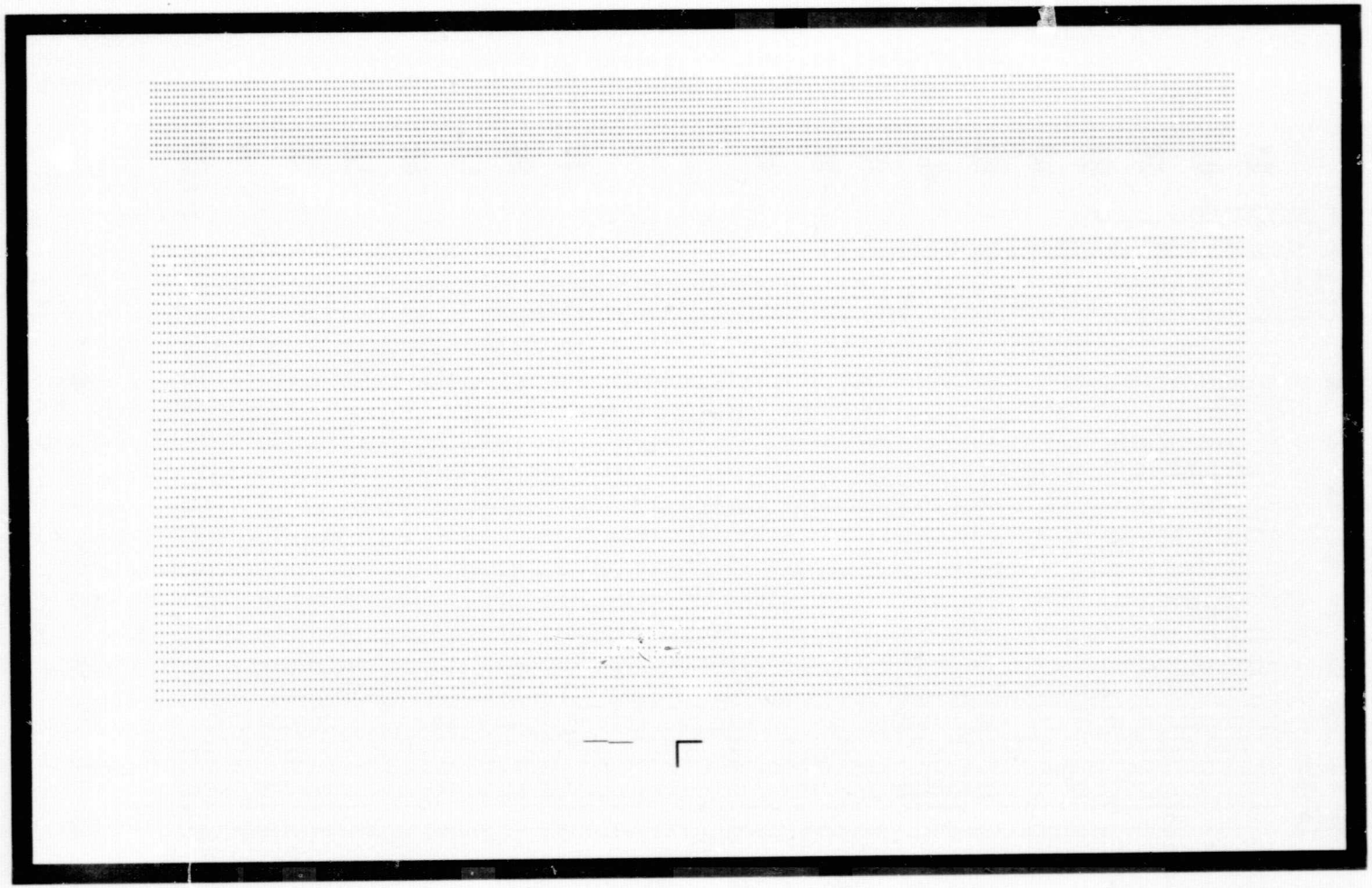

Figure 3. Contacts.

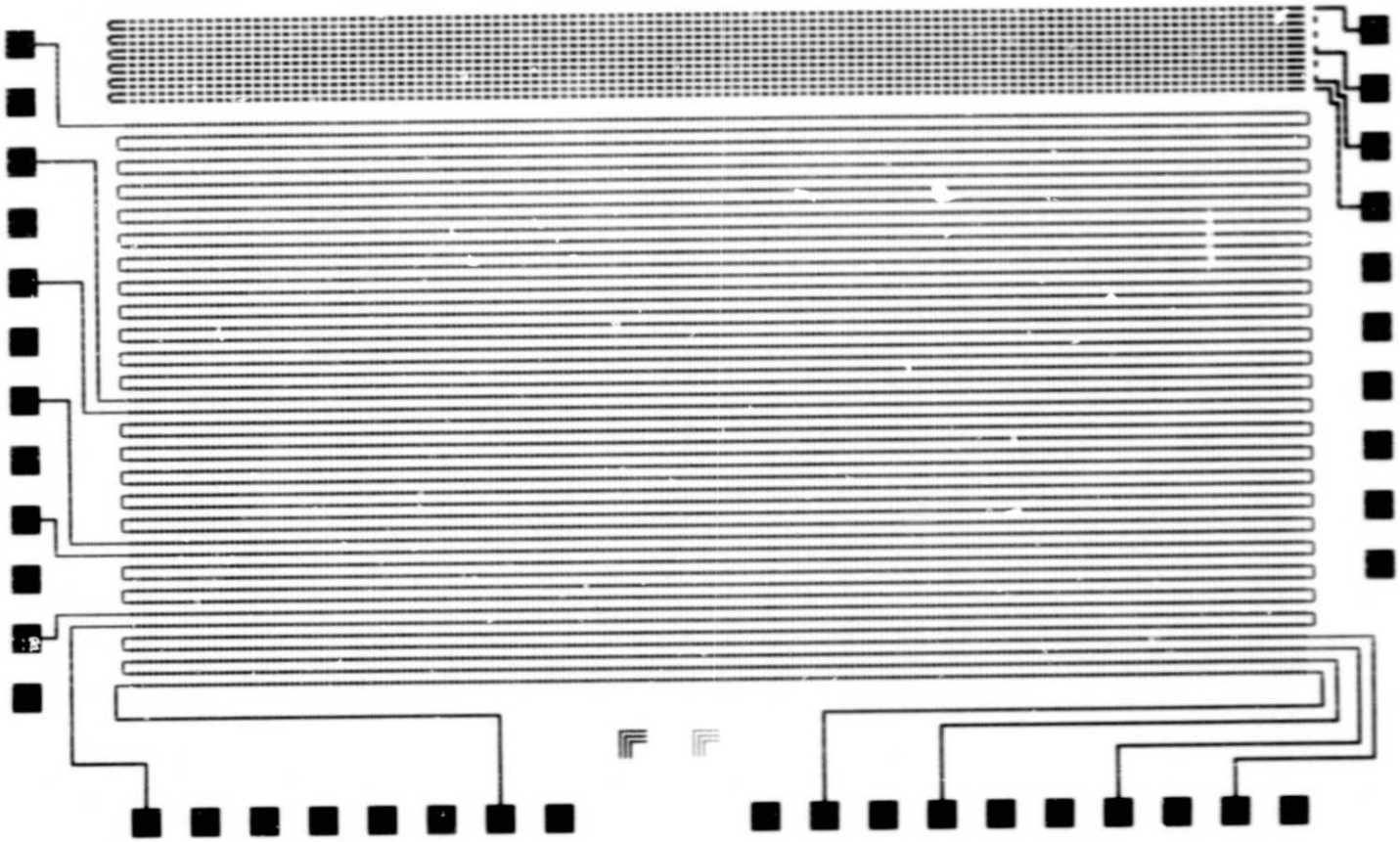

Figure 4. Metal pattern.

III. PAS PROCESS SEQUENCES

The standard CMOS/SOS deep-depletion silicon-gate process is shown in Fig. 5. The process begins with the deposition of 0.6 μm of (100) n-type silicon on ($\bar{1}102$) sapphire as described by Cullen (ref. 1). A layer of 3000 Å of SiO_2 is then deposited over the surface, and the silicon island pattern is defined in the oxide. Next, the silicon is etched using a KOH-n-propanol-H_2O solution, and the masking oxide is removed. The silicon islands are thermally oxidized at 900°C in steam to grow approximately 1000 Å of SiO_2. Using chemical-vapor-deposition techniques incorporating SiH_4 in H_2 at 700°C, 5000 Å of polycrystalline silicon is deposited. This is followed by a deposited SiO_2 layer containing enough boron to produce a silicon surface concentration of 1 to 5 x 10^{20} atoms per cm^3. The boron-doped SiO_2 layer is then etched to define the polycrystalline gate pattern, and the impurities are driven into the polysilicon at a temperature of 1050°C for 15 minutes in helium. After the diffusion, the boron glass is stripped in HF, and the undoped polysilicon is etched away in the KOH solution. The channel oxide is removed over the source and drain regions using a buffered HF solution, and a phosphorus-doped SiO_2 layer is deposited. This layer contains a phosphorus concentration sufficient to achieve a silicon surface concentration of 1-5 x 10^{19} atoms per cm^3. After this layer is defined over n-channel transistors, a second boron layer is deposited over the surface of the wafer. The silicon surface concentration obtainable from this second boron layer is 5-10 x 10^{19} atoms per cm^3. The impurities are next driven into the silicon film at 1050°C for 15 minutes in helium. Following an oxide anneal at 500°C for 15 minutes in hydrogen, the contacts are opened through the deposited oxides, 15,000 Å of aluminum is deposited, and the metal pattern defined. A 3000-Å layer of oxide is deposited on the surface of the wafer for scribe and break protection, the bond pads are opened in this oxide, and, finally, the metal is alloyed with the silicon at 425°C for 15 minutes in forming gas.

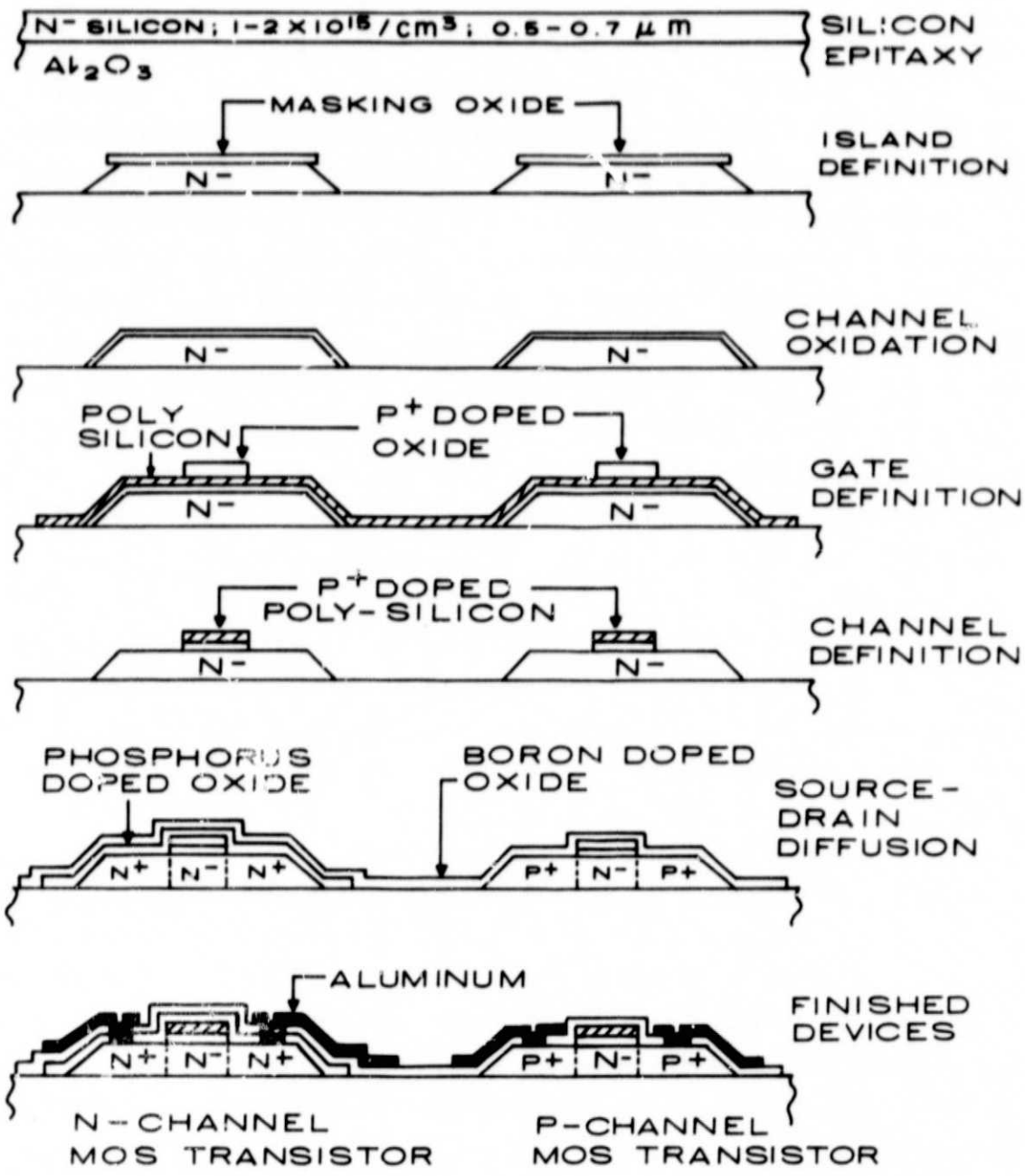

Figure 5. Standard CMOS/SOS deep-depletion silicon-gate process.

This process was originally described by Sarace and Ipri (ref. 2). It has been used for the fabrication of a wide variety of digital arrays (refs. 3 - 5), such as watch circuits (ref. 2), memories (ref. 3), and shift registers (ref. 6). The Process Analysis Structure will be used for a complete analysis of this process and of its interrelationship with the design rules presently being used with this process. There are several process sequences which can be used in conjunction with the PAS to analyze various individual process steps. Some of these sequences are described in detail below.

A. Process Sequence #1

1. General. - The first process sequence duplicates many of the actual fabrication steps shown in Fig. 5 and checks the following or determines their absence (e.g., short-circuits):

(1) silicon island continuity
(2) polysilicon over silicon island continuity
(3) polysilicon-silicon island short-circuits before channel oxide self-align etch
(4) (3) after channel oxide self-align etch
(5) (3) after source-drain diffusion
(6) metal over polysilicon-silicon island continuity
(7) metal to polysilicon short-circuits
(8) metal to silicon island short-circuits
(9) (3) after contact opening
(10) (3) after contact opening and metal deposition
(11) contact definition

2. Silicon Island Continuity. - The process sequence that will be used to study the integrity of the silicon islands will be:

(1) deposit 0.6-μm silicon on sapphire layers
(2) deposit 3000 Å of masking oxide
(3) define the masking oxide (Mask #1)

(4) etch the silicon island pattern (KOH) and strip the masking oxide

(5) deposit boron-doped SiO_2

(6) diffuse silicon islands (1050°C - 15 minutes - helium)

(7) strip boron-doped SiO_2

(8) electrically test (Test Sequence #1) for silicon island continuity

Once the integrity of the silicon islands is determined, the following process steps will be performed:

(9) grow channel oxide (900°C - 45 minutes - steam)

(10) deposit polycrystalline silicon (5000 Å)

(11) deposit boron-doped SiO_2

(12) define boron-doped glass (Mask #2)

(13) diffuse polysilicon (1050°C - 15 minutes - helium)

(14) strip boron glass

(15) etch away undoped polysilicon (KOH)

(16) open bond pad areas (Mask #5)

(17) electrically test for polysilicon continuity (Test Sequence #2)

(18) electrically test for polysilicon, silicon island short-circuits (Test Sequence #3)

(19) etch away channel oxide from source-drain areas (with buffered HF)

(20) electrically test (Test Sequence #3)

(21) deposit phosphorus and boron source-drain diffusion sources

(22) diffuse (1050°C - 15 minutes - helium)

(23) open bond pad areas

(24) electrically test (Test Sequence #3)

3. Metal Continuity and Short Circuits. - Next, the aluminum layer must be deposited and checked.

(1) deposit 1.5 μm of aluminum

(2) define metal pattern (Mask #4)

(3) electrically test for metal continuity (Test Sequence #4)

(4) electrically test for metal-polysilicon short-circuits (Test Sequence #5)

(5) electrically test for metal-island short-circuits (Test Sequence #6)

4. Contact Effects. - In the final group of tests, several chemical reactions and electrical tests are performed.

(1) strip metal (Caro's acid)

(2) define and etch contacts (Mask #3)

(3) electrically test for poly-island short circuits (Test Sequence #3)

(4) deposit 1.5 μm of aluminum

(5) define metal pattern (Mask #4)

(6) electrically test for poly-island or poly-metal short-circuits (Test Sequence #3)

(7) electrically test contact array (Test Sequence #7)

B. Process Sequence #2

This sequence is concerned only with the polysilicon and metal levels and checks for:

(1) planar polysilicon continuity

(2) metal over polysilicon continuity

(3) metal to polysilicon short-circuits

1. Polysilicon Continuity. -

(1) deposit 0.5 μm of polysilicon

(2) deposit boron-doped oxide (0.3 μm)

(3) define doped oxide (Mask #2)

(4) diffuse polysilicon (1050°C - 15 minutes - helium)

(5) strip boron glass (HF)

(6) etch away undoped polysilicon (KOH)

(7) electrically test for polysilicon continuity (Test Sequence #2)

(8) deposit phosphorus- and boron-doped glasses

2. Metal Continuity and Short Circuits. -

(1) deposit 1.5 μm of aluminum

(2) define and etch aluminum (Mask #4)

(3) electrically test for metal continuity (Test Sequence #4)

(4) electrically test for metal to polysilicon short-circuits (Test Sequence #5)

C. Process Sequence #3

This sequence is intended to determine the integrity of metal lines on a planar (sapphire) surface.

(1) deposit 1.5 μm of aluminum on a sapphire wafer

(2) define and etch the metal pattern (Mask #4)

(3) electrically test for metal continuity (Test Sequence #4)

In addition, the polysilicon mask or silicon island mask may be substituted in step (2) above. This will permit the evaluation of 0.2-mil metal patterns instead of the 0.4-mil metal pattern which is defined with Mask #4.

D. Process Sequence #4

It is the object of this process sequence to examine the integrity of the metal over silicon island crossovers. The sequence checks for:

(1) metal continuity over silicon island steps

(2) metal to silicon island short-circuits

1. Silicon Island and Metal. -

(1) 0.6-μm silicon films are deposited on sapphire substrates

(2) 0.3 μm of masking oxide is deposited

(3) the poly pattern is defined in the oxide (Mask #2)

(4) the oxide is etched (HF)

(5) the silicon islands are etched (KOH)

(6) the masking oxide is stripped

(7) phosphorus and boron oxides are deposited

(8) the silicon is diffused (1050°C - 15 minutes - helium)

(9) the probe pads are opened (Mask #5)

2. Metal Continuity and Short Circuits. -

(1) 1.5 μm of aluminum is deposited and defined (Mask #4)

(2) electrically test the silicon island continuity (Test Sequence #2)

(3) electrically test for metal continuity (Test Sequence #4)

(4) test for metal to silicon island short-circuits (Test Sequence #5)

E. Process Sequence #5

This sequence duplicates as closely as possible the fabrication sequence shown in Fig. 5. It does not permit the evaluation of several process steps which have been analyzed in previous sequences such as silicon island continuity, but useful results can be obtained. The sequence is:

(1) deposition of 0.6 μm of silicon on sapphire doped in the $1\text{-}2 \times 10^{15}/cm^3$ range

(2) definition and etching of the silicon island pattern (Mask #1)

(3) channel oxidation (900°C - 45 minutes - steam)

(4) polysilicon deposition, definition, and etching (Mask #2)

(5) channel oxide self-align etch

(6) doped oxide, source-drain diffusion source deposition

(7) source, drain diffusion (1050°C - 15 minutes - helium)

(8) open probe pads (Mask #5)

(9) If the sources and drains have been doped n+, then a positive bias on the polysilicon will produce a conducting channel in the silicon islands and, hence, it is possible at this stage to check for:

(a) silicon island continuity (Test Sequence #1)

(b) silicon island to polysilicon short-circuits (Test Sequence #3)

(c) polysilicon continuity (Test Sequence #2)

(10) deposit 1.5 μm of aluminum

(11) define and etch (Mask #4)

(12) electrically test for:

(a) metal continuity (Test Sequence #4)

(b) metal to polysilicon short-circuits (Test Sequence #5)

F. Summary

Five process sequences have been described which permit the evaluation of most of the individual fabrication steps in the present CMOS/SOS deep-depletion, silicon-gate process. It should be possible from these sequences to obtain the yield data for each individual process step in order to:

(1) ascertain if there exists a dominant yield-limiting process step

(2) build a complete process yield model from each individual process yield expression.

IV. PAS ELECTRICAL TEST SEQUENCES

This section describes in detail the test sequences that were alluded to in the various process sequences given in Section III.

A. Test Sequence #1

Verification of silicon island continuity as defined by the first mask level is the object of this test sequence. A voltage will be applied to one end of each silicon island string. The other end will be connected to system ground. The applied voltages are listed below:

Island Length (mils)	Voltage Applied (V)
200	+ 1.0
400	+ 2.0
600	+ 3.0
1200	+ 6.0
2400	+ 12.0
4800	+ 24.0

The current flow out of the power supply will be monitored, and the current flow value will be used to determine if the silicon island string is continuous or open, in addition to determining its resistance value.

B. Test Sequence #2

This sequence is similar to Test Sequence #1 and is designed to check the definition of Mask Level #2. The voltage applied as a function of polysilicon length is:

Polysilicon Length (mils)	Voltage Applied (V)
400	1.0
800	2.0
1200	3.0
2400	6.0
4800	12.0
9600	24.0

The current flow is again measured, and if it is less than 1.0 μA the line is assumed to be open. The resistance of the polysilicon line is also determined.

C. Test Sequence #3

This sequence is designed to test for short-circuits between Mask Level #1 (silicon islands) and Mask Level #2 (polysilicon). Both ends of the polysilicon line are connected to system ground while both ends of the silicon island are connected to a positive voltage that is a function of the silicon island length.

Silicon Island Length (mils)	Voltage (V)
200	1.0
400	2.0
600	3.0
1200	6.0
2400	12.0
4800	24.0

The current is again monitored, where 1.0 μA is the threshold that suggests the presence of a short-circuit. It should be noted that this test sequence increments the supply voltage. If the insulating layer between the two levels cannot withstand the applied voltages, then

this test sequence will not monitor the number of intrinsic short-circuits present but will simply indicate the breakdown voltage range.

D. Test Sequence #4

Due to the higher conductivity of metal array (Mask #4), a slightly different approach will be used to determine METAL continuity integrity. One end of the metal line will be connected to a 6-V power supply with the other end connected to ground through a 1-MΩ resistor. The current will again be measured with 1.0 μA as the current threshold.

E. Test Sequence #5

This sequence tests for short-circuits between Mask Level #2 and Mask Level #4. The applied voltages and current measuring are essentially the same as Test Sequence #3.

F. Test Sequence #6

Short-circuits are determined between Mask Level #1 and Mask Level #4. Again the supply voltages current monitoring are the same as Test Sequence #3.

G. Test Sequence #7

The continuity of the contact array will be tested by applying 10.0 V to one end of the string and connecting the other end to ground. The current flow will be monitored with 0.2 μA as the threshold voltage.

V. CONCLUSIONS

During this report period the mask set for the Process Analysis Structure was designed and digitized, and the initial artwork was done. Various process sequences were generated to permit evaluation of:

(1) planar silicon island continuity
(2) planar polycrystalline silicon continuity
(3) planar metal continuity
(4) nonplanar polysilicon continuity
(5) nonplanar metal continuity
    (a) metal over silicon islands
    (b) metal over polycrystalline silicon
    (c) metal over polycrystalline silicon which is crossing over silicon islands
(6) silicon island to polysilicon short-circuits
    (a) before channel oxide self-align etch
    (b) after channel oxide self-align etch
    (c) after source-drain diffusions
    (d) after contact etching
    (e) after metal definition
(7) silicon island to metal short-circuits
    (a) without poly-level present
    (b) with poly-level present
(8) polysilicon to metal short-circuits
    (a) without silicon island level present
    (b) with silicon island level present
(9) contact integrity

There are other process sequences described as well as sequences which have as yet to be envisioned. It is felt that familiarity with this test array will lead to several other process evaluation techniques incorporating this mask set and the basic concepts of process analysis described in the previous quarterly reports.

In addition, electrical test sequences have been described which can be programmed into most computer-controlled test sets to permit rapid data gathering. During the final period of this program, masks will be received, and wafers processed and tested to verify the procedures herein described.

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